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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/527,865	03/16/2005	Joan Wichard Strijker	NL 020904	9323

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EXAMINER	
MURALIDAR, RICHARD V	
ART UNIT	**PAPER NUMBER**
2838	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/527,865	STRIJKER, JOAN WICHARD	
	Examiner	Art Unit	
	Richard V. Muralidar	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *15* is/are allowed.

6)☒ Claim(s) *1-10 and 13* is/are rejected.

7)☒ Claim(s) *11,12 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/03/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figs. 1, 2, 3, and 8A should be labeled Prior Art since all that is disclosed is already known. Appropriate correction is required.

Empty boxes in the drawings should be labeled to enhance circuit readability and component recognition. For example, Fig. 1 box 160 should be labeled "oscillator", box 110 should be labeled "power control" etc. Appropriate correction is required.

Specification

The abstract of the disclosure does not commence on a separate sheet in accordance with 37 CFR 1.52(b)(4). A new abstract of the disclosure is required and must be presented on a separate sheet, apart from any other text. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

Claims 1-10, and 13 are rejected under 35 U.S.C. 102 as being unpatentable over the acknowledged prior art.

With respect to Claim 1, applicant's prior art [as disclosed in Figs. 8A and pages 13-14 of applicant's specification] teaches a leading edge blanking circuit [Fig. 8A] comprising: an input terminal [Fig. 8A input terminal to 150NOT] for receiving a trigger signal indicating a time at which a blanking period should

commence; switching means [Fig. 8A MOSFET 150 S2] arranged to be activated by the trigger signal to change from a first state to a second state; comparison means [Fig. 8A comparator 150 C2] having a first input terminal [Fig. 8A comparator 150 C2 positive terminal] being connected to a reference source [Fig. 8A reference voltage source U1], a second input terminal [Fig. 8A comparator 150 C2 negative terminal] arranged to receive a voltage which ramps over time in response to the trigger signal and an output terminal [Fig. 8A comparator 150 C2 output terminal] for providing an output signal of the leading edge blanking circuit which changes state subsequent to the voltage at the second terminal of the comparison means reaching the voltage level supplied by the reference source to the first terminal; and a charging circuit [Fig. 8A constant current source I1 with capacitor 150 Ct] for providing the ramp voltage to the second input terminal of the comparison means, the circuit being characterized in that the time taken for the ramp voltage to reach the voltage level supplied by the reference source [applicant's specification page 13 lines 30-31] is variable [see below] and dependent upon a control signal.

The applicant's improvement over the existing prior art of "adaptive leading edge blanking circuits" has been interpreted to be encompassed only by the variable time required for the ramp voltage to match the reference source in comparator 150 C2, whereas the prior art provides for a more or less constant time [applicant's specifications page 14 lines 23-32]. The prior art constant time is in fact not always constant if one considers that current sources are only constant over a given operating range and not one exact value of current. Any movement within the range of acceptable current values will automatically result

in a variable time for the ramp voltage to match the reference source. Additionally, every time the MOSFET 150 S2 switches, there will be a measurable time period required for the current from the current source to go from zero to its full operating range, which will also result in variability. Additionally, the prior art circuit as shown in Fig. 8A is fully capable of causing a variable time required for the ramp voltage to match the reference source in comparator 150 C2 if one simply varies the current flowing into current source I1, or varies the voltage reference level of U1, by any of a number of well known means in the art. The suggestion to do this is provided in applicant's disclosed prior art by Burgyan [US 6219262], which shows a comparator [Fig. 5A Is comp] that has its reference input adaptively switched by a transistor with current sensing means, so as to produce a variable time required for the input voltage to match the reference source in comparator Is comp.

Functional language will be given the appropriate amount of patentable weight when the described circuit/device can be interpreted as simply being capable of performing the function, instead of actually performing the function.

With respect to Claim 2, applicant's prior art [as disclosed in Figs. 8A and pages 13-14 of applicant's specification] teaches the reference voltage supplied to the first terminal of the comparison means comprises the control signal [Fig. 8A both terminals can be said to receive control signals].

With respect to Claim 3, applicant's prior art [as disclosed in Figs. 8A and pages 13-14 of applicant's specification] teaches that the charging circuit comprises a current source and a capacitor [applicant's specification page 14 lines 1-2; Fig. 8A current source I1 and capacitor 150 Ct], the current source

being arranged to charge the capacitor following an initiation of change in state of the switching means from the first state to the second state and, wherein, the voltage supplied to the second input terminal of the comparison means is arranged to ramp in accordance with a charged state of the capacitor [page 14 lines 12-22].

With respect to Claim 4, applicant's prior art [as disclosed in Figs. 8A and pages 13-14 of applicant's specification] teaches that the switching means comprises a transistor switch [Fig. 8A transistor 150 S2], the charging circuit comprises a capacitor connected in parallel with the transistor switch [Fig. 8A capacitor 150 Ct] and a current source [Fig. 8A current source I1] arranged to charge the capacitor when the transistor switch is not in the first state, the comparison means comprises a comparator [Fig. 8A comparator 150 C2], wherein the first terminal is a non-inverting input [Fig. 8A 150 C2 positive terminal] and the second terminal is an inverting input [Fig. 8A 150 C2 negative terminal], the first terminal being connected to the control signal and the second terminal being connected to a terminal of the charging circuit at a point between the current source and the capacitor [as shown in Fig. 8A].

With respect to Claim 5, applicant's prior art [as disclosed in Figs. 8A and pages 13-14 of applicant's specification] teaches the reference voltage supplied to the first terminal of the comparison means is a fixed voltage reference source [Fig. 8A reference voltage source U1] and, wherein, the control signal is arranged to vary a current level in the charging circuit, to change the rate at which the voltage at the second input terminal of the comparison means

ramps over time [Fig. 8A- varying the rate of switching of transistor 150 S2 accomplishes this].

With respect to Claim 6, applicant's prior art [as disclosed in Figs. 8A and pages 13-14 of applicant's specification] teaches that the charging circuit comprises a voltage source [Fig. 8A current source I1 is a recognized equivalent of a voltage source with a resistor in series], a transistor [Fig. 8A transistor 150 S2] and a capacitor [Fig. 8A capacitor 150 Ct], the transistor being responsive to the voltage source and the control signal to turn on and to supply a charging current to the capacitor.

With respect to Claim 7, applicant's prior art [as disclosed in Figs. 8A and pages 13-14 of applicant's specification] teaches the charging current to the capacitor is a variable current, dependent upon a potential difference between the voltage source and the control signal [since sources are only constant over a given operating range and not to one exact value, the charging current to the capacitor will likewise vary. Additionally, every time the MOSFET 150 S2 switches, there will be a measurable time period required for the current from the current source to go from zero to its full operating range, which will also result in variability.

With respect to Claim 8, applicant's prior art [as disclosed in Figs. 8A and pages 13-14 of applicant's specification] teaches the first switching means comprises a transistor switch [Fig. 8A transistor 150 S2; the comparison means comprises a comparator [Fig. 8A comparator 150 C2] in which the first terminal comprises a non-inverting terminal connected to a fixed voltage reference source [Fig. 8A reference voltage source U1], and the second input terminal

comprises an inverting input; and the charging circuit comprises a capacitor [capacitor 150 C2], transistor [transistor 150 S2 is also a part of the charging circuit since the charge and discharge of capacitor 150 C2 directly depends upon its switching action] and a voltage source [Fig. 8A current source I1- current sources are easily interchangeable with voltage sources and vice versa, particularly since the reference U1 is already a voltage reference], the capacitor being connected in parallel with the first switching means and having one terminal thereof connected in common to the inverting input of the comparator and an output terminal of the transistor, the transistor being arranged to supply a variable current from the voltage source dependent upon a voltage level of the control signal supplied to its control input [control signal at the input of 150NOT accomplishes this by controlling the switching action of transistor 150 S2].

With respect to Claim 9, applicant's prior art teaches a power controller for a switched mode power supply for supplying a control signal to a leading edge blanking circuit of claim 1, the power controller being arranged to output the control signal at a substantially constant level during a first operating power range of the SMPS and, in a second operating power range to progressively decrease the level of the control signal as the output power requirements of the SMPS decrease [this is a functional description of voltage regulation theory of operation and is the normal means of operation for a switched mode power supply, as shown in prior art Fig. 1].

With respect to Claim 10, applicant's prior art teaches the first range of operating power range comprises a normal operating power range of the SMPS

being controlled, and the second range comprises a low power to very low power operating range [this is a functional description of voltage regulation theory of operation and is the normal means of operation for a switched mode power supply, as shown in prior art Fig. 1].

With respect to Claim 13, applicant's prior art teaches a switch mode power supply including a flyback converter comprising a power controller [as shown in prior art Fig. 1] arranged to set a desired power output of the SMPS by generating a control signal "trip level" [trip level signal available from power control 110] at which the SMPS is to revert from an on-power state to an off-power state, a switch controller [latch 170] for controlling a main switching component [switch S110] of the SMPS in accordance with the power requirements as set by the "trip level" signal and a leading edge blanking circuit [prior art Fig. 8A] for providing an output signal "blank" arranged to validate or inhibit resetting of the switch controller, wherein the leading edge blanking circuit comprises a leading edge blanking circuit according to claim 1.

Allowable Subject Matter

Claims 11-12 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 15 is allowable.

The following is a statement of reasons for the indication of allowable subject matter: Claim 11 is allowable over the art of record because the prior art

does not teach a control output terminal for supplying a timer level control signal output terminal connected to the supply voltage via a first biasing means and to one terminal of the transistor, in combination with the other limitations of Claim 11.

Claim 12 is allowable over the art of record because the prior art does not teach an output terminal of the amplifier connected to a first terminal of the transistor, the transistor connected to a second output terminal of the power controller and a second terminal of the first bias resistor, in order to provide the timer level control signal to the second output terminal.

Claim 14 is allowable over the art of record because the prior art does not teach the leading edge blanking circuit has a timer level signal that is a constant voltage regardless of the actual trip level and that decreases once the trip level decreases below the threshold level.

Claim 15 is allowable over the art of record because the prior art does not teach that a reduced level reference voltage is provided to the voltage controlled switch of the leading edge blanking circuit to adaptively reduce the leading edge blanking period in a low to very low operating power range of the SMPS

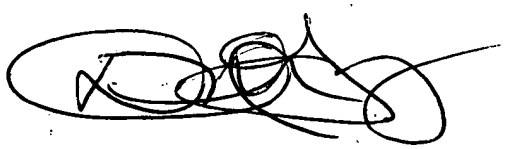
The limitations of Claims 11-12 and 14-15 are not anticipated or rendered obvious by the prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard V. Muralidar whose telephone number is 571-272-8933. The examiner can normally be reached on Monday to Friday 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Gray can be reached on Monday to Friday 8-5. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



DAVID M. GRAY
PRIMARY EXAMINER

RVM
04/03/2006